CLAIMS

1. A telecommunications encoder for converting synchronous data to asynchronous data, the encoder comprising:

a signal processor configured to process signals to perform tasks on portions of collected synchronous data and to output asynchronous, packetized data; and

control logic, associated with the signal processor, configured to initiate performance of tasks by the signal processor at respective start times of the tasks and configured to control collection of synchronous data based on run times of the tasks such that collection of synchronous data for a given task is completed approximately at the start time of the given task.

2. The encoder of claim 1 wherein the control logic is configured to control the signal processor to collect data for a second task, to be performed next after a first task, during operation of the first task.

3. The encoder of claim 1 further comprising a co-processor coupled to the signal processor and configured to prioritize the tasks and to determine start times of the tasks depending on priorities of the tasks.

4. The encoder of claim 3 wherein the co-processor is configured to assign latency-critical functions to different tasks.

5. The encoder of claim 4 wherein the co-processor is configured to assign latency-critical functions of equal processing periods to tasks of equal priority.

6. The encoder of claim 1 wherein the signal processor comprises a DSP and the control logic comprises a DSPOS.

7. The encoder of claim 1 wherein control logic comprises software.

8. The encoder of claim 1 wherein the control logic is configured to maintain a plurality of counters each associated with a signal processor task.

9. The encoder of claim 8 wherein the control logic is configured to decrement the counters for each task and to request that a task be run when its corresponding counter reaches a given value.

10. A telecommunications decoder for converting asynchronous data to synchronous data, the decoder comprising:

a co-processor configured to provide asynchronous data packets upon request;

a signal processor coupled to the co-processor and configured to perform tasks on asynchronous, packetized data received from the co-processor and to output synchronous data; and

control logic configured to cause the signal processor to send a data request to the co-processor in response to a start time of a task for processing data from the co-processor, being at or within a data request offset from a current time.

11. The decoder of claim 10 wherein the data request offset is greater than an amount of time from when the data request is sent to the co-processor from the signal processor to when the data are received by the signal processor from the co-processor in response to receiving the data request.

12. The decoder of claim 10 wherein the logic is further configured to maintain a plurality of task counters.

13. The decoder of claim 12 wherein the logic has an associated frequency and is configured to decrement the task counters each cycle of the logic.

14. The decoder of claim 13 wherein the logic is configured to cause the signal processor to send the data request when a task counter equals the data request offset.

15. The decoder of claim 14 wherein the data request offset is less than approximately 1ms longer than an amount of time from when the data request is sent to the co-processor from the signal processor to when the data are received by the signal processor from the co-processor in response to receiving the data request.

16. The decoder of claim 14 wherein the co-processor is configured to control data request offsets for tasks.

17. A digital signal processor for use in a telecommunications system, the processor comprising:

a plurality of stored telecommunication data queues;

data processing circuitry configured to perform a plurality of telecommunication functions, the circuitry being configured to access the data queues to store output data from the first function in a first queue and to take data to process by a second function from a second data queue; and

logic configured to control the data processing circuitry to transfer data from the first queue to the second queue for use by the second function;

wherein the data queues, the data processing circuitry, and the logic are disposed on a common processing chip.

18. The digital signal processor of claim 17 wherein the logic is configured to transfer data from the first queue to multiple data queues.

19. The digital signal processor of claim 17 wherein the plurality of data queues include output queues and input queues and the logic includes the output queues and one or more of the input queues.

20. The digital signal processor of claim 19 wherein the logic includes a digital signal processor operating system (DSPOS) configured to control the processing circuitry to periodically transfer approximately i seconds of data from a first output queue to a first input queue in accordance with a relationship between the first input queue and the first output queue included in the logic.

21. The digital signal processor of claim 20 wherein the relationships are stored in a 2-dimensional table indicative of data output queues and associated data input queues.

22. The digital signal processor of claim 21 wherein the DSPOS periodically traverses the table approximately every i seconds, and wherein i equals 0.001.

23. The digital signal processor of claim 17 wherein a digital signal processor operation system periodically transfers a portion of data from the first queue to the second queue.